5.7.3 Design for Test Parameters The following other considerations are important to the general land pattern design that should be incorporated into the printed board:

a) Two non-plated tooling holes should be available on diagonal corners of the printed board.
b) Test lands should be 2.5 mm [0.0984 in] minimum from the edge of the printed board to facilitate gasketing on vacuum fixtures.
c) When using vias for test points, caution should be taken to insure that signal quality is not degraded at the expense of testing capability.
d) Test lands should be 0.63 mm [0.0248 in] minimum from mounting land areas.
e) Where possible, provide numerous test lands for power and ground.
f) Where possible, provide test lands for all unused gates. Free running gates sometimes cause instability during in-circuit testing. This will provide a means of grounding these spurious signals.

It is sometimes desirable to provide drive and sense nodes test lands to perform six-wire bridge measurements during in-circuit test. Directions for this should come from test engineering.

In addition, it is useful to identify the test vias and lands on an assembly drawing in event of the need to modify the circuit topology. Changes made without moving test lands avoid fixture modification, saving cost and time.

Care should be taken when mounting components on the secondary side to avoid covering a via hole that is a designated test land. Also, if a via hole is too close to any component, damage may result to the component or fixture during probing (see Figure 5-3).

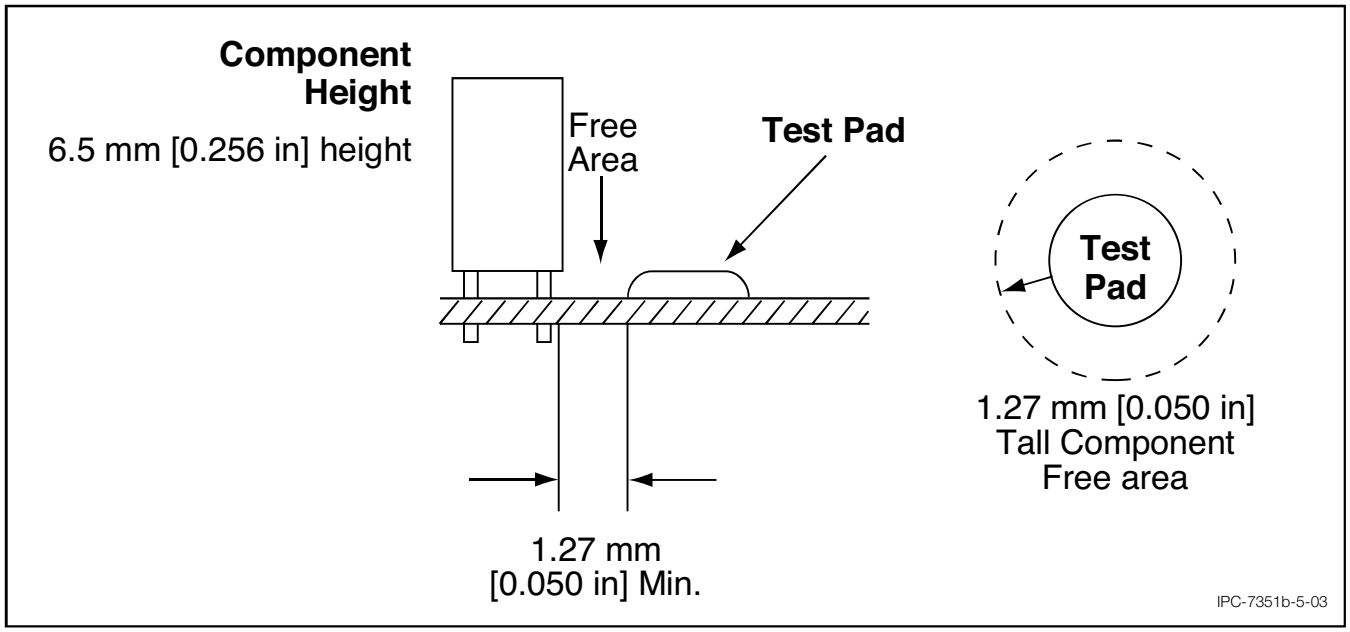

Figure 5-3 Test Probe Feature Distance from Component

6 PRINTED BOARD STRUCTURE TYPES

The selection of a printed board structure for surface mounting applications is important for optimum thermal, mechanical and electrical systems reliability. Each candidate structure has a set of properties with particular advantages and disadvantages when compared to others (see Table 6-1).

It is probable that no one printed board structure will satisfy all of the needs of the application. Therefore, a compromise of properties should be sought that offers the best ‘‘tailoring’’ for component attachment and circuit reliability.

Table 6-1 Printed Board Structure Comparison

Type	Major Advantages	Major Disadvantages	Comments
Organic Base Substrate Epoxy fiberglass	Substrate size, weight, rework-able, dielectric properties, conventional printed board processing.	Thermal conductivity, X, Y and Z axis CTE.	Because of its high X-Y plane CTE, it should be limited to environments and applications with small changes in temperatures and/or small packages.
Polyimide fiberglass	Same as epoxy fiberglass plus high temperatures X-Y axis CTE, high Tg.	Thermal conductivity, Z-axis CTE, moisture absorption.	Same as epoxy fiberglass.
Epoxy aramid fiber	Same as epoxy fiberglass, X-axis CTE, lightest weight.	Thermal conductivity, Z-axis CTE, resin microcracking, Z axis CTE, water absorption.	Volume fraction of fiber can be controlled to tailor X-Y CTE. Resin selection critical to reducing resin micro-cracks.
Polyimide aramid fiber	Same as epoxy aramid fiber, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, Z-axis CTE, resin microcracking, water absorption.	Same as epoxy aramid fiber.
Polyimide quartz (fused silica)	Same as polyimide aramid fiber, X-Y axis CTE.	Thermal conductivity, Z-axis CTE, drilling, availability, cost, low resin content required.	Volume fraction of fiber can be controlled to tailor X-Y CTE, drill wear-out higher than with fiberglass.
Fiberglass/aramid composite fiber	Same as polyimide aramid fiber, no surface microcracks, Z axis CTE.	Thermal conductivity, X and Y axis CTE, water absorption, process solution entrapment.	Resin microcracks are confined to internal layers and cannot damage external circuitry.
Fiberglass/PTFE® laminates	Dielectric constant, high temperature.	Same as epoxy fiberglass, low-temperature stability, thermal conductivity, X and Y axis CTE.	Suitable for high-speed logic applications. Same as epoxy fiberglass.
Flexible dielectric	Light weight, minimal concern to CTE, configuration flexibility.	Size, cost, Z-axis expansion.	Rigid-flexible printed boards offer trade-off compromises.
Thermoplastic	3-D configurations, low high-volume cost.	High injection-moulding setup costs.	Relatively new for these applications.
Nonorganic Base Alumina (ceramic)	CTE, thermal conductivity, conventional thick film or thin film processing, integrated resistors.	Substrate size, rework limitations, weight, cost, brittle, dielectric constant.	Most widely used for hybrid circuit technology.
Supporting Plane Printed board bonded to plane support (metal or nonmetal)	Substrate size, reworkability, dielectric properties, conventional printed board processing, X-Y axis CTE, stiffness, shielding, cooling.	Weight.	The thickness/CTE of the metal core can be varied along with the printed board thickness, to tailor the overall CTE of the composite.
Sequential processed board with supporting plane core	Same as printed board bonded to supporting plane.	Weight.	Same as printed board bonded to supporting plane
Discrete wire	High-speed interconnections, good thermal and electrical features.	Licensed process, requires special equipment.	Same as printed board bonded to low-expansion metal support plane.
Constraining Core Porcelainized copper-clad invar	Same as alumina.	Reworkability, compatible thick film materials.	Thick film materials are still under development.
Printed board bonded with constraining metal core	Same as printed board bonded to low expansion metal cores, stiffness, thermal conductivity, low weight.	Cost, microcracking.	The thickness of the graphite and printed board can be varied to tailor the overall CTE of the composite.
Compliant layer sructures	Substrate size, dielectric properties, X-Y axis, CTE.	Z-axis CTE, thermal conductivity.	Compliant layer absorbs difference in CTE between ceramic package and substrate.

6.1 General Considerations Printed board structures vary from basic printed boards to very sophisticated supporting-core structures. However, some selection criteria are common to all structures. To aid in the selection process, Table 6-2 lists design parameters and material properties which affect system performance, regardless of printed board type. Also, Table 6-3 lists the properties of the materials most common for these applications.

Table 6-2 Printed Board Structure Selection Considerations

Design Parameters	Material Properties								
	Transition Temperatures	Coefficient of Thermal Expansion	Thermal Conductivity	Tensile Modulus	Flexural Modulus	Dielectric Constant	Volume Resistivity	Surface Resistivity	Moisture Absorption
Temperatures and power cycling	X	X	X	X					
Vibration				X	X				
Mechanical shock				X	X				
Temperatures and humidity	X	X				X	X	X	X
Power density	X		X						
Chip carrier size		X		X					
Circuit density						X	X	X	
Circuit speed						X	X	X	

Table 6-3 Printed Board Structure Material Properties

Material	Material Properties							
	Glass Transition Temperature	XY Coefficient of Thermal Expansion	Thermal Conductivity	XY Tensile Modulus	Dielectric Constant	Volume Resistivity	Surface Resistivity	Moisture Absorption
Unit of Measure	°C	PPM/°C (Note 4)	W/M°C	PSI x 10^{-6}	At 1 MHz	Ohms/cm	Ohms	Percent
Epoxy fiberglass	125	13-18	0.16	2.5	4.8	10^{12}	10^{13}	0.10
Polyimide fiberglass	250	12-16	0.35	2.8	4.8	10^{14}	10^{13}	0.35
Epoxy aramid fiber	125	6-8	0.12	4.4	3.9	10^{18}	10^{16}	0.85
Polyimide aramid fiber	250	3-7	0.15	4.0	3.6	10^{12}	10^{12}	1.50
Polyimide quartz	250	6-8	0.30		4.0	10^{9}	10^{8}	0.50
Fiberglass/ PTFE	75	20	0.26	0.2	2.3	10^{10}	1011	1.10
Thermoplastic resin	190	25-30		3-4	10^{17}	10^{13}	N/A	
Aluminaberyllia	N/A	5-7 21.0	44.0	8.0	10^{14}			
Aluminum (6061 T-6)	N/A	23.6	200	10	N/A	10^{6}		N/A
Copper (CDA101)	N/A	17.3	400	17	N/A	10^{6}		
Copper-clad Invar	N/A	3-6	150XY/20Z	17-22	N/A	10^{8}		N/A

Note 1. These materials can be tailored to provide a wide variety of material properties based on resins, core materials, core thickness, and processing methods.
Note 2. The X and Y expansion is controlled by the core material and only the Z axis is free to expand unrestrained, where the Tg will be the same as the reinforced resin system used.
Note 3. When used, a compliant layer will conform to the CTE of the base material and to the ceramic component, thereby reducing the strain between the component and the printed board.
Note 4. Figures are below Tg, and are dependent on method of measurement and percentage of resin content.

6.1.1 Categories In general, a printed board structure will fit into one of four basic categories of construction: organic base material, nonorganic base material, supporting plane, and constraining core.

6.1.2 Thermal Expansion Mismatch A primary concern when using low expansion surface mount parts is the thermal expansion mismatch between the leadless part and the printed board structure. This mismatch will fracture solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures. The number of fatigue cycles before solder joint failure depends on the thermal expansion mismatch between the part and the printed board structure, the temperature range over which the assembly must operate, the solder joint thickness, the size of the part and the power cycling. For example, power cycling may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between a device or package and the printed board structure.

6.2 Organic-Base Material Organic-base materials work best with leaded chip carriers. With leadless chip carriers and some BGA packaging, the thermal expansion mismatch between package and substrate can cause problems. Also, flatness, rigidity, and thermal conductivity requirements may limit their use. Finally, attention should be paid to package size, I/O count, thermal cycling stability, maximum operating temperature and solder joint compliance.

6.3 Nonorganic Base Materials Nonorganic ceramic base materials typically used with thick-or thin-film technology, although more costly, are suited for leaded and leadless chip carrier designs. Suppliers can incorporate thick-or thin-film resistors directly on the ceramic structure and buried capacitor layers that increase density and improve reliability. However, repairability of the printed board structure is limited. Ceramic materials, usually alumina, appear ideal for printed board structure with leadless ceramic chip carriers because of their relatively high thermal conductivity. Unfortunately, the structure is limited to approximately 100 mm square. Ceramic printed board structures have three primary applications: ceramic hybrid circuits, ceramic multi-chip modules (MCM-L) and ceramic printed boards.

6.4 Alternative Printed Board Structures

6.4.1 Supporting-Plane Printed Board Structures Supporting metallic or nonmetallic planes can be used with conventional printed boards or with custom processing to enhance printed board properties. Depending on the results desired, the supporting plane can be electrically functional or not and can also serve as a structure stiffener, heatsink and/or CTE constraint.

6.4.2 High-Density Printed Board Technology High-density, sequentially processed, multilayer printed board structures are available in a wide variety of organic dielectrics. Using thinner copper foils for fabrication the printed board manufacturer can provide very narrow conductor and spacing features and by implementing smaller mechanical drills, laser ablation, photo-lithography or plasma processes, smaller blind and/or buried vias can be provided for layer-to-layer interconnections.

The major advantage of this system is that the vias can be as small as 0.10 mm [0.00394 in] or less and conductor widths can range from below 0.12 mm [0.00472 in] for high interconnection density. Thus, some applications can be satisfied with fewer signal layers while providing additional layers for power and ground. Refer to IPC-2226 for more detailed design guidelines for high density printed boards.

6.4.3 Constraining Core Structures As with supporting plane, one or more supporting metallic or nonmetallic planes can serve as a stiffener, heatsink, and/or CTE constraint in constraining core structures.

6.4.4 Porcelainized Metal (Metal Core) Structures An integral core of low-expansion metal (for example, copper-clad Invar) can reduce the CTE of porcelainized metal structures so that it closely matches the CTE of the ceramic chip carrier. Also, the structure size is virtually unlimited. However, the low melting point of the porcelain requires low-firing-temperature conductor, dielectric and resistor inks.

7 ASSEMBLY CONSIDERATIONS FOR SURFACE MOUNT TECHNOLOGY (SMT)

The smaller size of surface mount components and the option of mounting them on one or both sides of the printed board structure significantly reduces printed board real estate. The type of SMT assembly is basically determined by the type of surface mount components to be used; see 7.1 for a description of types and classes.

7.1 SMT Assembly Process Sequence The SMT assemblies are soldered by reflow (infrared, hot air convection, laser, conduction, vapor phase, and/or wave soldering processes) depending upon the mix of surface mount and through-hole mount components. The process sequence for one-sided SMT is shown in Figure 7-1. Solder paste is applied, components are placed, the assembly is reflow soldered and cleaned. For two-sided SMT assemblies, the printed board is turned over and the process sequence just described is repeated. The assembly process for two-sided SMT is simply a sequential combination of SMT processes, however, component weight vs. surface tension should be calculated to determine if heavy components will require additional reinforcement prior to the second reflow soldering process.

The process sequence for surface mount with through-hole component technology is shown in Figure 7-2. Adhesive is applied and the surface mounted components placed. The adhesive is then cured, and the printed board is inverted to receive the through-hole component leads automatically or by hand insertion. After lead clinching (if required), and with the through-hole components on top and the surface mount components beneath, the printed board is typically wave soldered. An alternative sequence is to reverse the initial stages i.e., insert (and clinch) the through-hole components before attaching the surface mounted components and then wave soldering.

Finally the assembly may be cleaned, inspected, repaired if necessary, and tested, though not necessarily in that order.

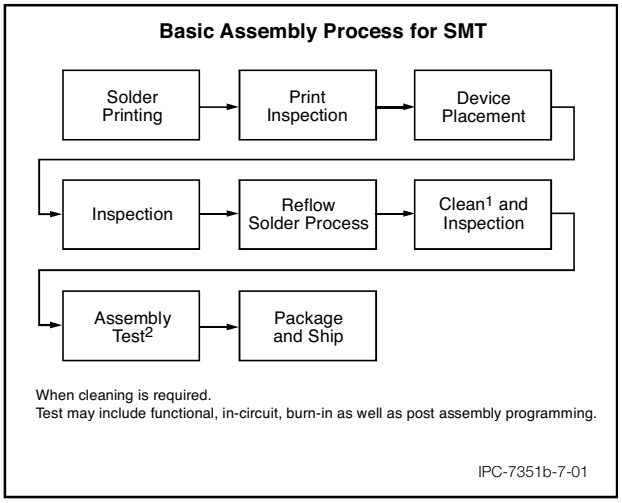

Figure 7-1 Typical Process Flow for One-Sided SMT

7.2 Substrate Preparation

7.2.1 Adhesive Application In wave soldering surface mount components, selection and application of adhesive plays a critical role. With too much adhesive, the adhesive flows onto lands resulting in poor solder fillets. Too little adhesive will fail to accomplish its objective of holding parts to the bottom of the printed board during wave soldering.

7.2.2 Conductive Adhesive Some applications for SMT attachment use conductive adhesive as the attachment material. Unlike solder paste which is redistributed when reflowed, conductive adhesives must be properly controlled to ensure joint strength. Also, component placement must be controlled in order to prevent excessive adhesive squeeze-out, and possible shorts to adjacent lands.

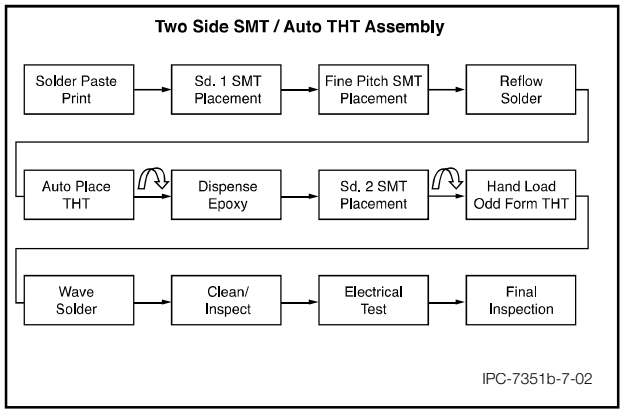

Figure 7-2 Assembly Process Flow for Two-Sided Surface Mount with THT

7.2.3 Solder Paste Application Solder paste plays an important role in reflow soldering. The paste tacks the component before reflow. It contains flux, solvent, suspending agent, and alloy of the desired composition. Solder paste is applied on the lands before component placement either by screening, stenciling, or syringe. Screens are made from stainless steel or polyester wire mesh, and stencils are etched stainless steel, brass, and other stable alloys. Stencils are preferred for high-volume applications. They are more durable than screens, easier to align, and can be used to apply a thicker layer of solder paste, and, where narrow, point apertures are required for example, for fine-pitch lands. Electroformed stencils may be required for very small components such as 0201 capacitors and resistors.

The goal of the technology that's employed to make the stencil is to ensure that this transfer is as efficient and complete as possible. There are several post processes that enhance the stencil's performance, including electropolishing and trapezoidal section apertures that are created with laser cut technology.

7.2.3.1 Laser Cut Stencil Development Laser cut stencils are produced directly from the customer's original Gerber file or IPC-2581 data. Eliminating the need to make a photo tool eliminates the potential for misregistration. And since there are no photographic steps, a stencil can be made with excellent positional accuracy and remake reproducibility. The tolerance on the aperture dimensions can be held to 7 µm [276 µin], allowing for printing 0.3 mm [0.0118 in] pitch. This process yields maximum paste release, resulting in minimal stencil cleaning, thereby increasing printing efficiency. Plus, the laser cutting process inherently creates trapezoidal apertures, furthering complete paste transfer.

A trapezoidal section aperture is one which has a larger opening on the contact (printed board) side of the stencil than on the squeegee side. The opening on the contact side is typically 5 µm [197 µin] per side larger than the squeegee side dimension, depending on the customer's requirements. This wall geometry, when further enhanced by electropolishing, allows for better paste release during the printing process. The results are more noticeable on fine pitch components.

Depending on the overall array design and given the right metal thickness selection, chem-etched stencils can perform adequately at 0.5mm [0.0197 in] pitch. Their efficiency can be improved with performance enhancing processes such as electropolishing and/or trapezoidal section apertures. For more details in the engineering of the stencil for specific soldering requirements, refer to IPC-7525.

7.2.4 Solder Preforms Solder preforms are sometimes used for through-hole mounted devices as well as SMT rework or prototype boards. They come in specific size and composition, with flux either inside the preforms, or as a coating or without flux. They may be cost-effective to avoid wave solder processes if there are only a few leaded components on the printed board.

7.3 Component Placement The accuracy requirements for device placement make it more practical to use robotically controlled machines for surface mount components on the printed board. Selection of the appropriate autoplacement machine is dictated by the type of components to be placed and the assembly production rate. Sequential placement equipment typically utilizes a software controlled X-Y moving table system. Components are individually placed on the printed board in succession. Typical cycle times vary with component size and complexity.

7.3.1 Component Data Transfer Prior to designing the printed board in the CAD system, each component is constructed in digital form creating an electronic database. The CAD data is most often used to prepare photo-tool artwork, printed board fabrication details and assembly instructions but, if developed in the correct format, it can also be adapted to manufacturing processes. Direct transfer of CAD data into automated assembly systems will accelerate production set-up and reduce overall assembly system programming time.

When the CAD database for the device is prepared, specific physical data for each device can be used to assist assembly machine programming for both component placement (X-Y coordinate position) and orientation. To facilitate the X-Y coordinate information, a datum position must be established on the printed board surface. The recommended datum "0" for X and Y coordinates ideally, may be one of the global fiducial targets at the lower left or lower right corner of the printed board or panel. Surface mount devices are furnished in tape and reel as well as tube magazine feeders to accommodate high-speed assembly systems (tray carriers are most often adapted for fine-pitch components).

Each surface mount device is aligned using the body center and a starting orientation for reference. "0" degree is the basic orientation of the device.

Rotational data must be specified from the "0" position in a counter-clockwise direction (typically 90° - 180° - 270°). The "0" starting position of the component is significant. Tape and reel and JEDEC tray packaged devices for example, have an established standard for orientation.

The tape-and-reel packaged devices have a predetermined orientation that is related to the perforated pattern on one edge of the embossed tape carrier. The standard orientation does vary, however, between unique device families.

Passive and active devices are supplied in a tape and reel format, held and protected within an embossed pocket. Each device family or package type has a standard orientation in relation to the perforated indexing pattern at the tape edge.

Orientation as well as polarity of a device must be defined in the CAD database if the output transferred to assembly systems is to be reliable. Resistors and capacitor devices are common in orientation and have no defined polarity. As the designer develops the component database, numbers are typically assigned to each end of the device to accommodate circuit routing and maintain orientation of value marking or polarity. Tantalum capacitors, diodes, ICs and other polarized components, for example, have unique orientation in relation to tape feed systems. Consider the relationship of the device orientation within the tape cavity to perforation at the tape carrier material edge.

7.4 Soldering Processes Like the selection of automated placement machines, the soldering process selection depends upon the type of components to be soldered and whether or not they will be used in combination with leaded parts. For example, if all components are surface mount types, reflow method (vapor phase, hot air convection or infrared) may be desirable. However, for through-hole and surface mount combinations, in mixed technology, a combination of wave soldering and reflow soldering may be used. No process is best for all soldering tasks. In addition, the number of soldering processes discussed in the following text are by no means complete.

7.4.1 Wave Soldering Wave soldering is an economical method of soldering mass terminations. There are five to six main process variables that must be controlled in the wave soldering process: fluxing, preheat, conveyor speed, conveyor incline, solder temperature, and possibly cooling rate.

In preheat, allowance in the conveyer system must be made for the thermal expansion of the board during preheating and soldering to prevent printed board warpage.

In fluxing, flux density, activity and flux foam/flux spray/ flux wave height must be closely monitored. A system must be in place to determine when the flux activity has deteriorated and when the old flux must be replaced and the new flux added.

Speed is the time sequence and duration of all of the steps in soldering. By controlling the speed, more uniform and better joints result. In controlling the conveyer speed, preheating a packaging and interconnecting assembly in two or three stages minimizes the thermal shock damage to the assembly and improves its service life. Uniform preheating is achieved by developing a solder schedule that specifies preheat settings and conveyer speed for each type of printed board.

The solder wave is an important variable. Wave geometry is especially important for preventing icicles and bridges and for the proper soldering of surface mounted components. Wave geometries include uni-directional and bi-directional; single and double; rough, smooth and dead zone; oil intermix, dry, and bubbled, and with or without a hot air knife. Special solder waves just for surface mounted components are also available.

The concern generally expressed in wave soldering of surface mount devices is damage to the components when they go through the soldering wave at 260 °C [500 °F]. The maximum shift in tolerance of resistors and capacitors is generally found to be 0.2%. This is a negligible amount considering the part tolerance of commonly used components is 5% to 20%. The components generally spend about three seconds in the wave but they are designed to withstand soldering temperatures of 260 °C [500 °F] for up to ten seconds.

In wave soldering, outgassing and solder skips are two other main concerns. The outgassing or gas evolution occurs on the trailing terminations of chip resistors and capacitors. It is believed to be caused by insufficient drying of flux and can be corrected by raising the packaging and interconnecting assembly preheat temperature or time. The other concern, solder skips, is caused by the shadow effect of the part body on the trailing terminations. Orienting the part in such a way that both terminations are soldered simultaneously solves most shadow effect problems. Some manufacturers use an extra land to serve as a "solder thief" for active components.

The most common method for solving both outgassing and shadow effect is by switching to the dual wave system where the first wave is turbulent and the second wave is laminar. The turbulent wave serves to provide an adequate amount of solder across the surface of the packaging and interconnecting structure in order to help eliminate outgassing and solder skips. The laminar wave is used to help eliminate icicles and bridging.

7.4.2 Vapor Phase (VP) Soldering Vapor phase soldering, also known as condensation soldering, uses the latent heat of vaporization of an inert liquid for soldering. The latent heat is released as the vapor condenses on the part to be soldered. The soldering temperature is constant and is controlled by the type of fluid.

Unlike wave, IR, convection and laser soldering, vapor phase soldering does not require control of the heat input to the solder joints or to the printed board. It heats independently of the part geometry, heats uniformly, and does not exceed the fluid boiling temperature. This process is also suitable for soldering odd-shaped parts, flexible circuits, pins and connectors, and is also suitable for reflow of tin-lead electroplate and surface mount packages. Since heating is by condensation, the rate of temperature rise depends on the mass of the part. Therefore, the leads on the package in contact with the packaging and interconnecting structure heat up faster than the component body. This may lead to wicking of the solder up the lead. Before exposing the loaded assembly to VP reflow process, preheating the assembly is highly recommended to avoid thermal shock to components and the printed board.

7.4.3 IR Reflow Soldering In infrared (IR) reflow soldering, the radiant or convective energy is used to heat the assembly. There are basically two types of IR reflow methods, either focused (radiant) or non-focused (convective). The latter is proving more desirable for SMT. The focused IR radiates heat directly on the parts and may unevenly heat assemblies. The heat input on the part may also be color-dependent. In non-focused or diffused IR, the heating medium can be air or an inert gas or simply the convection energy. A gradual heating of the printed board assembly is necessary to drive off volatiles from the solder paste. After an appropriate time in preheat, the assembly is raised to the reflow temperature for soldering and then cooled.

7.4.4 Hot Air/Gas Convection Soldering The reflow process affects soldering by transporting the printed boards through a stream of heated gas (e.g., air, nitrogen). Heat is transferred to the components and printed board by conduction from the gas. Because the printed boards do not receive significant direct radiation from the heating source, convection soldering avoids the shadowing problems that can occur with infrared soldering machines, especially short wavelength (lamp) versions. This enables more uniform heating and a higher component density on the printed board compared to other mass reflow soldering methods. The gas temperature controls the maximum temperature that can be seen by the assembly.

Use of a nitrogen atmosphere permits better thermal coupling between the circulating gas and the component terminations. In addition to improved wetting, the process window for double-sided reflow is enlarged, and lower activated solder paste flux can be used.

7.4.5 Laser Reflow Soldering Laser soldering complements other mass soldering processes rather than replacing them and, as with in-line reflow soldering, lends itself well to automation. It is faster than hand soldering but not as fast as wave, vapor, IR soldering or hot air convection. Heat-sensitive components that may be damaged in reflow processes can be soldered by laser. Process problems include thermal damage to surrounding areas and solder balls.

7.4.6 Conduction Reflow Soldering Conduction reflow affects soldering through the transference of heat from beneath the printed board. This can have advantages with high mass components, temperature sensitive components and metal backed assemblies. In comparison with other solder processes, the slightly slower heating and cooling ramp times caused by heat spreading through the printed board substrates can provide a reduction of thermal shock and improved resistance against rapid cooling issues such as tombstoning. Though in-line conduction reflow ovens are available, the most common use of conductive reflow is in "hot plate" rework systems.

For more detail regarding reflow soldering refer to IPC-7530.

7.5 Cleaning Flux requiring solvent cleaning—synthetic or rosin-based fluxes are generally known as synthetic activated (SA), synthetic mildly activated (SMA), rosin activated (RA) or rosin mildly activated (RMA). Stabilized halogenated hydrocarbon/alcohol azeotropes are the preferred solvents for removal of synthetic and rosin-based flux residues.

7.6 Repair/Rework The repair/rework of surface mount assemblies requires special care in design and practice. Because of the small land geometries, heat applied to the printed board should be minimized. There are various tools available for removing components. Resistance heating tweezers are usually used for removing surface mounted components. Various types of hot air/gas and IR systems are also used for removing surface mounted components. One of the main issues when using hot air/gas devices is preventing damage to adjacent components. Refer to IPC-7711/21. There are four basic requirements for a successful rework; good printed board design layout, selection of the correct rework equipment or tools, sufficient manual skill, and adequate training.

Successful removal of large multi-leaded integrated circuit packages involves the use of hot gas or heated electrode tools. Sufficient clearance around the package to permit the re-work is essential. Clearance should be provided completely around the device as identified in 3.1.5.4 as the "courtyard manufacturing zone."

7.6.1 Heatsink Effects Large ground planes or heatsinks will conduct heat away from the component being reworked if present in a printed board substrate. Extra heat, perhaps for longer periods, is then required which, in turn, can lead to damage to components or the board. The fact that the solder joints may not reach reflow temperature is no guarantee that the component or the printed board have not been overheated. Heatsinking effects is a design problem which must be tackled at the printed board layout stage. Whenever possible, any component termination which may not rework, including leaded-through hole type, should be thermally isolated from any ground plane or integral heat-sink by a short length of copper conductor.

7.6.2 Dependence on Printed Board Material Type To ensure minimum damage to the printed board during rework, base laminate should be a good quality resin and reinforcement type from a high copper peel strength material. High packing density is required. The use of inferior laminates can easily lead to problems with lands peeling away during rework. This may result in either scrapping of complete assemblies or expensive repair of damaged copper area. For printed boards having high thermal mass such as middle-core types or those with large area ground planes, to avoid employing a tool with high heat input rate, the use of a hot plate to provide background heating is essential.

7.6.3 Dependence on Copper Land and Conductor Layout When the space on a printed board is at a premium or single conductors must be kept very short, a conductor may be placed between adjacent device land space at a pitch of the component device being placed. In such cases, conductors should be covered with a solder mask to minimize the risk of lifting conductors during rework operations.

Routing conductors between lands at 1.0 mm pitch and below increases the risk of damage to the conductors during the rework operation. For more detail regarding development, planning and trouble shooting the steps involved in the process of producing surface mount assemblies, refer to IPC-S-816.

8 IPC-7352 DISCRETE COMPONENTS

Discrete components are generally purchased in 8.0 mm and 12.0 mm wide tape and reel (see Figure 8-1). EIA-481 is the applicable specification for tape and reel. Consult your manufacturers guide for the packaging availability of your component.

Parts susceptible to damage by electrostatic discharge **shall** be supplied in a manner that prevents such damage. Tape peel strength **shall** be 40 ± 30 grams. Peel from the top for the top cover of the tape. Reel materials used in the construction of the reel **shall** be easily disposable metal, chip board, styrene plastic or equivalent. Reels **shall** not cause deterioration of the components or their solderability. Reels must be able to withstand high humidity conditions.

Parts must be capable of withstanding cleaning processes currently used by board assem bly manufacturers. This may include as a minimum four-minute exposures to solvent cleaning solutions at 40 °C [104 °F], plus a minimum of a one-minute exposure to ultrasonic immersion at a frequency of 40 kHz and a power of 100 watts per square foot. Alkaline systems in use **shall** also not damage parts or remove markings.

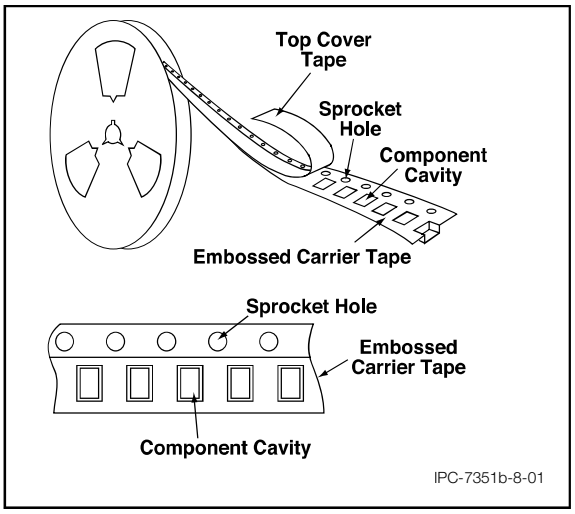

Figure 8-1 Packaging of Discrete Components

End terminations **shall** be coated with a finish that provides protection and maintains solderability. Evaluations of terminations **shall** use the methods described in IPC-J-STD-002. Test B/B1 and Test D **shall** be used as a default, unless AABUS. The user and supplier will need to agree on the coating durability requirements as defined in IPC-J-STD-002. If this is not provided, Typical Coating Durability Category 3 from IPC-J-STD-002 becomes the default condition for the surface finishes as shown in Table 8-1.

Table 8-1 Solderability Tests for Discrete Components

Test B/B1 of J-STD-002	Test D of J-STD-002	Steam Aging Default
Solder Bath/Dip and Look Test (Leadless Components)	Resistance to Dissolution/Dewetting of Metallization Test	Category 3-8 hours ± 15 min. Steam Conditioning

Plating may consist of a tin/lead alloy or a lead free equivalent. If tin/lead is used the solder should contain between 58 to 68% tin. Any coating may be applied to the termination by hot dipping or by plating from solution. Plated terminations should be subjected to a post plating reflow operation to fuse the solder. If tin/lead finish is used it should be at least 0.0075 mm [0.0003 in] thick.

The termination **shall** be symmetrical, and **shall** not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination **shall** cover the ends of the components, and **shall** extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes **shall** have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

The following sections for each component family provide information on basic component construction, termination materials, marking, carrier package format and resistance to soldering.

8.1 Chip Resistors (RESC) A variety of values exist for resistors. This section describes the most common types.

8.1.1 Basic Construction The resistive material is applied to a ceramic substrate and terminated symmetrically at both ends with a "wrap around" metal U-shaped band. The resistive material is face-up, thus trimming to close tolerances is possible. Since most equipment uses a vacuum-type pickup head, it is important that the surface of the resistor is made flat after trimming, otherwise vacuum pickup might be difficult (see Figure 8-2).

8.1.2 Marking Resistors equal to or larger than 2012 [0805] are labeled. Resistors smaller than 2012 [0805] are generally unlabeled.

8.1.3 Carrier Package Format Bulk rods, 8.0 mm tape/4.0 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

8.1.4 Resistance to Soldering Process Temperatures Parts should be capable of withstanding five cycles through a standard reflow system. Each cycle **shall** consist of 10 to 30 seconds or 20 to 40 seconds within 5 ºC of peak temperature for tin/lead or lead free, respectively.

Parts must also be capable of withstanding a minimum duration immersion in molten solder at the time and temperature shown in Table 8-2. If a reflow process is used the requirements of IPC/JEDEC J-STD-020 shows the appropriate reflow cycles and profiles for the reflow conditions as shown in Table 8-3.

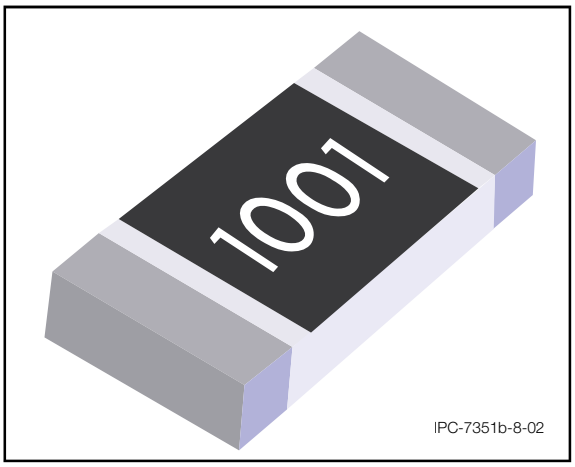

Figure 8-2 Chip Resistor Construction

Table 8-2 Solderability, Bath Method: Test Severities (duration and temperature)

Alloy Composition	Severity					
	(215 +/- 3) °C (3+/ 0.3)s	(10+/- 1)s	(235 +/- 5) °C (2+/ 0.2)s	(5+/- 0.5)s	(245 +/- 5) °C (3+/ 0.3)s	(250 +/- 5) °C (3+/ 0.3)s
SnPb	X	X	X	X		
Sn96.5Ag3.0Cu0.5					X	
Sn99.3Cu0.7						X

Alloy composition for test purposes only. The solder alloys consist of 3.0 wt% to 4.0 wt% Ag, 0.5 wt% to 1.0 wt% Cu, and the remainder of Sn may be used instead of Sn96.5Ag3.0Cu0.5. The solder alloys consist of 0.45 wt% to 0.9 et% Cu and the remainder of Sn may be used instead of Sn99.3Cu0.7

Note 1. "X" denotes "applicable'
Note 2. Refer to IPC-J-STD-006 to identify alloy composition
Note 3. The basic lead free solder alloys listed in this table represent compositions that are currently preferred for lead free soldering processes. If solder alloys other than those listed here are used, it should be verified that the given severities are applicable.

Table 8-3 Package Peak Reflow Temperatures

Reflow Conditions	Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm^3	Pkg. Thickness <2.5 mm and Pkg. Volume <350 mm^3
Tin/Lead Eutectic	Convection 225 +0/-5°C	Convection 240 +0/-5°C
Lead Free	Convection 245 +0 °C	Convection 260 +0 °C

Note 1. Package volume excludes external terminals (balls, bumps, lands, leads) and or non-integral heat sinks.
Note 2. The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMT packages may still exist.
Note 3. Components intended for use in a "lead-free" assembly process **shall** be evaluated using the "lead free" peak temperature and profiles defined.

8.2 Chip Capacitors (CAPC) A variety of values exist for capacitors. This section describes the most common types.

8.2.1 Basic Construction Multilayer ceramic capacitors use substrate materials such as alumina for hybrid circuits and porcelainized metal. The monolithic construction used in producing these chips results in a solid block of ceramic with an enclosed electrode system and metallized ends for circuit attachment. This solid block is rugged and capable of withstanding the harsh environment and treatment associated with manufacturing processes (see Figure 8-3). Electrodes are given a common terminal by coating the chip ends with a precious metal-glass formulation suspended in an organic vehicle. Consecutive drying and firing eliminates the organic components and affects a bond between the ceramic dielectric and glass constituent in the termination.

8.2.2 Marking Ceramic capacitors are typically unmarked.

8.2.3 Carrier Package Format Bulk rods, 8.0 mm tape/4.0 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.