a feeder overcurrent element (50) that, on detection of a feeder fault, sends a blocking signal to 50B (the bus overcurrent element). For a bus fault, no blocking action occurs, and the scheme operates after a short coordination delay. The coordination delay, t_C, as shown in Figure 36, allows the blocking signal to be received before bus tripping can occur. A blocking signal dropout timer, t_E, is used to prevent unwanted tripping due to the feeder overcurrent element dropping out faster than the bus overcurrent element. This blocking extension timer can include a small pickup delay, t_{PU}, in case the feeder relay asserts momentarily due to induction motor contribution.

A pickup setting for this scheme attempts to find an optimum point between security and dependability. The most downstream pickup optimum point may be near 50% of the maximum available fault current. For upstream coordination, a 20% to 30% security margin may be applied; this would place the pickup between 60% to 70% of the available fault current.

Timers for this scheme attempt to find an optimum point between speed and security. If different relays are used for the incomer and the radial feeders, the engineer may investigate the relay operate time. Also, the model of the relay may impact the blocking time as some contacts operate in microseconds (high-speed contacts) while others can be as slow as 12 ms. Using auxiliary relays increases blocking delay and, therefore, needs to be avoided. Lastly, the relay receiving a blocking signal may have settable debouncing timers. If set fast (i.e., below 4 ms), they may introduce unwanted blocking; if set slow, they would increase the tripping time. Ultimately, the timer choice impacts the arc flash energy levels.

An example of coordination timer, t_C, calculation follows:

$$t_C = t_{DIF} + t_{OP} + t_{DB} + t_{AUX} + t_{PU} + t_M \tag{9}$$

where

t_{DIF} is the difference of relay operation speed
t_{OP} is the contact closure time
t_{DB} is the debounce time of the upstream relay
t_{AUX} is the operate time of the interposing auxiliary relay(s) when used
t_{PU} is the pickup delay
t_M is the security margin

A typical timer is set between 33 ms and 133 ms.

A blocking signal may be implemented using contact outputs from the feeder relays to drive an input of the bus relay or via a communication channel provided communication signals have adequate operating speed and reliability for protection applications.

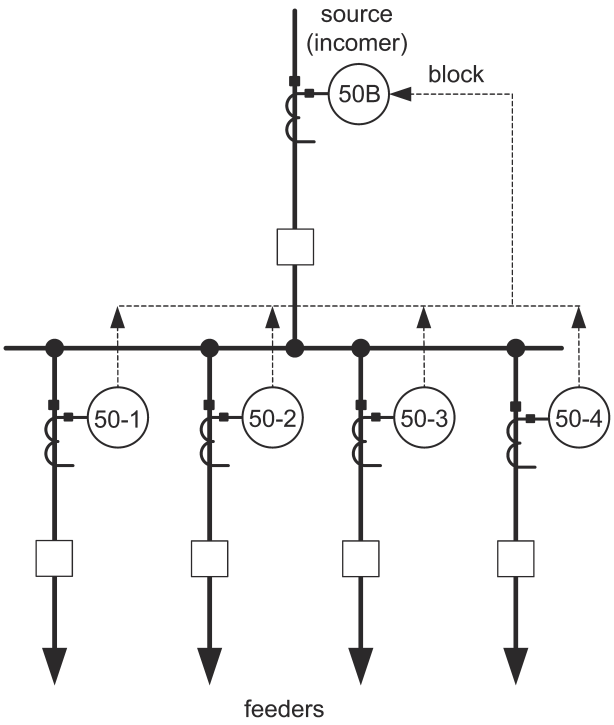

Figure 35—Radial blocking zone-interlocked scheme for a single bus with a single source

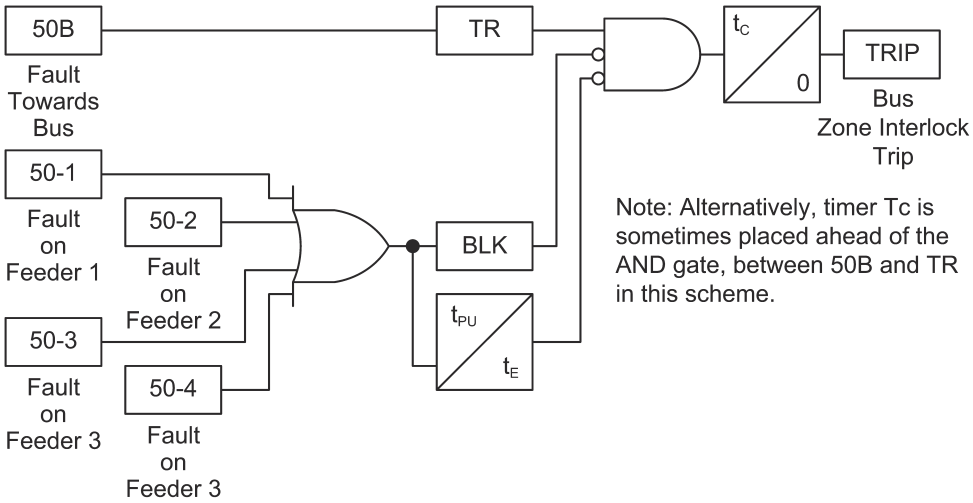

Figure 36—Radial blocking zone-interlocked scheme logic diagram

Radial blocking zone-interlocked schemes may also be used where there are multiple sources feeding a bus. In that case, the bus protection overcurrent element, 50B, essentially represents a partial differential scheme. The partial differential scheme measures only the sum of the source currents with the non-source feeder elements providing the blocking signals. The station arrangement depicted in Figure 37 is shown using directional tripping and blocking elements on the sources. As an alternate approach for applying a radial blocking zone-interlocked scheme for this arrangement, the source CTs and the bus tie breaker CTs can be connected in a partial differential scheme to the source relay making it naturally only responsive to faults toward the bus and

feeders. With this approach, a CT is required on each side of the bus tie breaker for overlapping zones, but no additional relay is needed on the bus tie breaker and all relays can be non-directional.

Radial blocking zone-interlocked schemes may also be used on some switchable (reconfigurable) bus arrangements. Relay logic or manual switches may be used to select which blocking signals are applied to the bus overcurrent element based on the present bus configuration.

The bus overcurrent element, 50B, pickup can be set above maximum expected load current and selected with adequate sensitivity and margin to detect any bus fault with a system outage(s) that provides a weak source condition. In many cases, this can be accomplished using a phase overcurrent element. In cases where additional ground fault sensitivity is required, a separate 50B ground overcurrent element can be added to the scheme.

Feeder overcurrent element, 50, pickup can be set lower than the associated bus overcurrent element by a small margin. If applied, the ground overcurrent elements are coordinated considering that feeder loads may include grounded-wye connected transformers, which can be a significant source of zero-sequence currents. The feeder relays can sense zero-sequence currents for a bus ground fault, and the pickup setting of the feeder ground overcurrent element may have to be increased to avoid picking up for a fault on the bus. However, if this is not possible, a directional ground element (67N) may be required on some of the outgoing feeders.

This scheme is primarily designed for radially connected load. Any condition on the outgoing feeders that can provide backfeed to the (faulted) bus can cause the scheme to operate improperly, typically, by blocking for an internal fault. Potential sources of backfeed can include distributed energy resources (DER) and regenerative load (such as large induction or synchronous motors) connected to one or more feeders.

It may be possible to set a pickup of the feeder blocking overcurrent element above any anticipated backfeed (for a small connected DER) or to employ directional overcurrent elements. The latter option is similar to the scheme depicted in Figure 37, but with the directional overcurrent elements applied to the outgoing feeders as well as to the incoming sources.

Note that, utilizing microprocessor-based multifunctional relays, this scheme may be built in conjunction with a conventional time-overcurrent bus protection scheme coordinated with the source (incomer) and feeder relaying. In such a design, even if a feeder should incorrectly block the scheme for an internal fault, it would still trip on the (slower) unsupervised time overcurrent elements.

7.3.3 Directional blocking zone-interlocked schemes

For radial buses with a single source and a predetermined short-circuit current flow, blocking zone-interlocked schemes can be implemented with non-directional overcurrent relays. More complex bus arrangements, with multiple sources and several patterns of short-circuit current flows, require directional overcurrent relays.

Figure 37 shows a typical substation layout with two sources (S1 and S2) feeding outgoing radial feeders from a two-section bus (Bus 1 and Bus 2) with a bus tie breaker (TB). Often, for this bus arrangement, an overcurrent relay is installed at the bus tie breaker. For selectivity, the bus tie breaker's relay has to be delayed to coordinate with the feeder relays and the main breakers' relays have to be delayed to coordinate with the bus tie breaker's relay. This significantly slows tripping for an internal bus fault. A blocking zone-interlocked scheme using directional relays with signaling logic can provide tripping with only a short signaling delay.

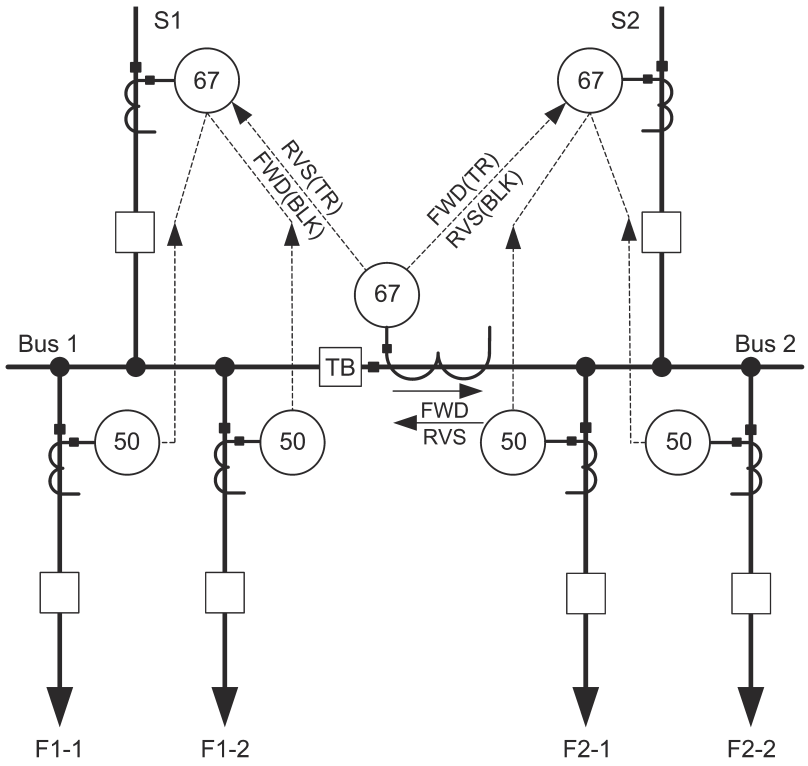

Figure 37—Bus blocking scheme for a dual-source, sectionalized bus

For this scheme, any source breaker would operate based on the directional overcurrent element to assert the tripping logic for a fault toward the bus and assert the blocking logic for a fault away from the bus. Radial feeders can be non-directional and used only for blocking as they do not assert for faults on the bus.

The logic for the directional blocking zone-interlocked scheme can be summed up as follows. If any relay senses a fault toward the bus and no relay senses a fault away from the bus, a trip is issued after a short delay to allow for signaling time from the blocking relays. Figure 38 shows the logic for Bus 1 and Bus 2. This logic could reside in the main or bus tie breaker's relay, or partial differential relay, or in a logic processor that aggregates the various tripping (fault toward the bus) and blocking (fault away from the bus) signals from the network element relays. In Figure 37, the logic resides in the relays on the main breakers. Since the directional tripping elements use voltage for directionality, a switch onto fault (SOTF) logic can be used to provide dependability when using bus VTs and energizing a faulted bus. Similarly, if the network element relays are connected to line-side VTs, the SOTF logic can be used to provide security when energizing a faulted network element that requires directional supervision.

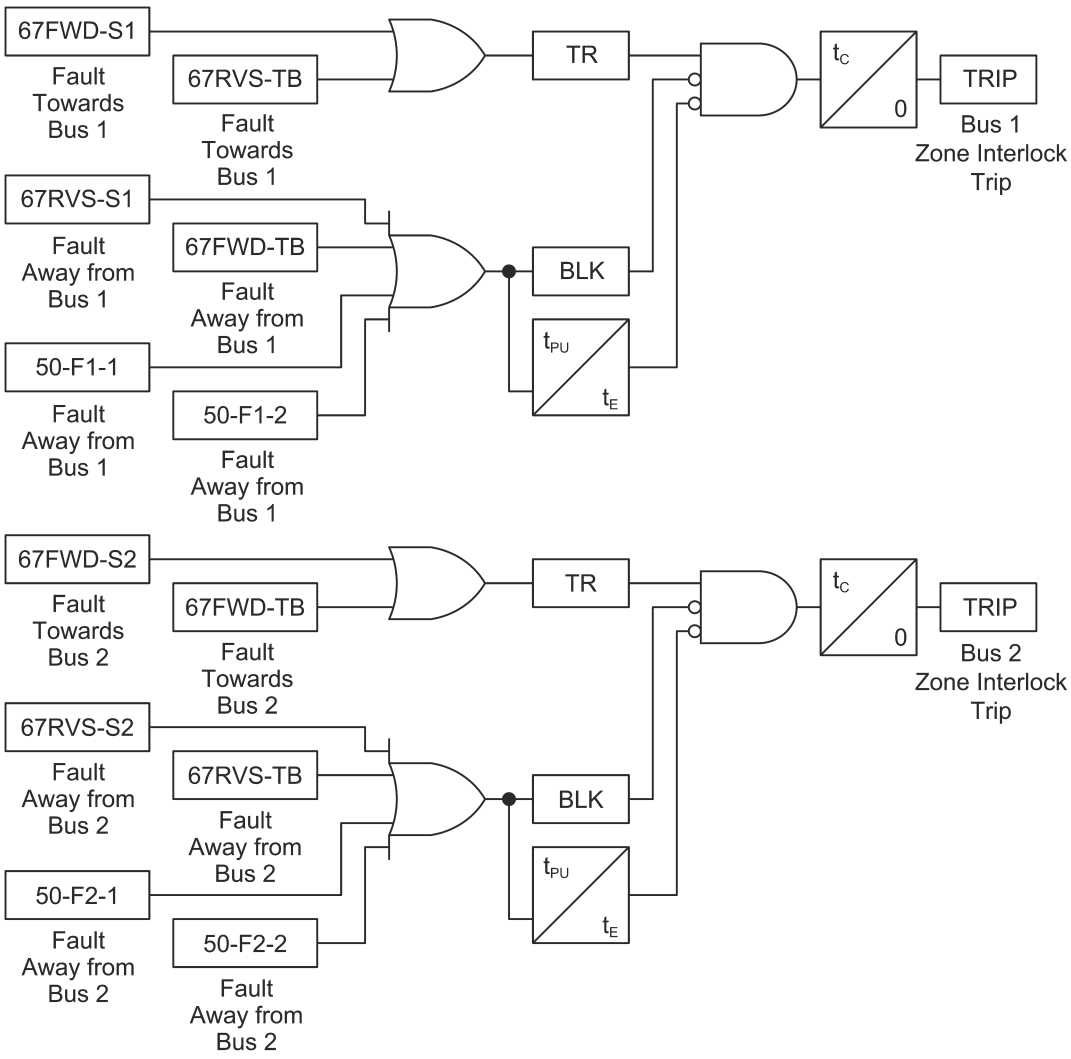

Figure 38—Trip logic for application of Figure 37 (PKP = non-directional overcurrent condition, FWD = forward direction, REV = reverse direction)

The scheme is suitable for straight buses where the network element relays can determine whether a fault is toward the bus to be protected. Thus, it is not suitable for application with dual-breaker arrangements, such as breaker-and-a-half or double-bus, double-breaker.

Positions of CTs define boundaries of zones of protection. Normally, feeder zones commence on the bus side of the breakers while the bus zone terminates on the line side of the breakers. Bus blocking zone-interlocked schemes violate this principle and do not allow for zones overlapping. Feeder application typically takes precedence, and the bus-side CTs are used in the bus blocking schemes.

Also, blocking zone-interlocked schemes provide for nearly instantaneous, but still slightly delayed, fault clearing times. Therefore, for applications demanding high performance of bus protection, differential schemes can be used for speed and selectivity. However, this scheme is a possible way to provide a second high-speed bus protection scheme if CTs are not available to implement dual differential schemes for redundancy. It does not require additional CTs and relays over those already used for network element protection.

7.3.4 CT requirements

Blocking zone-interlocked schemes are relatively immune to CT errors, including saturation. Given applied relay settings, the following three considerations are important to observe for checking CT ratings:

- Tripping functions are required to be dependable for all internal faults given the assumed sensitivity objectives. Typically, pickup levels are set above full load to prevent the scheme from being armed permanently, but below the minimum bus fault current. Normally, the setting is relatively low and the scheme faces no dependability problems even under severe saturation of CTs. In cases of very high fault currents and low-ratio CTs, such as in medium voltage industrial grids, special attention is required (see Linders et al. [B45]). The amount of secondary current may be considerably reduced due to severe CT saturation jeopardizing dependability of the tripping or blocking overcurrent functions.
- Blocking functions are required to be dependable for all external faults for which the tripping functions pick up. Severe saturation may reduce the apparent secondary current seen by the relay and jeopardize the security of the scheme. This, again, may be a problem if very low-ratio CTs are used. Typically, the tripping function is powered from a large ratio CT and does not have problems picking up on external faults while the blocking function powered from a low-ratio CT may fail to pick up, or pick up late after the coordination timer expires, leading to inadvertent operation of the scheme.
- Directional functions, if used, are required to retain directionality under CT errors. The fundamental frequency component in secondary current could shift due to CT saturation. Various implementations of directional functions could respond differently to saturated waveforms. In particular, negative-sequence or neutral overcurrent directional functions may be especially affected by CT saturation.

Typically, all three requirements—dependability of the tripping functions for bus faults, dependability of the blocking functions on external faults, and directional integrity—are satisfied even under considerable CT saturation, imposing no extra requirements for the CT. Typically, CTs properly rated for protection of circuits originating at the bus are sufficient for deployment of the bus blocking zone-interlocked scheme.

More stringent CT requirements apply if a given blocking zone-interlocked scheme is not based on phase overcurrent functions but on neutral or negative-sequence functions. These derived signals exhibit much higher sensitivity to faults and allow protecting buses in impedance-grounded systems and/or under very weak infeed conditions. However, CT errors can cause relays to measure spurious neutral and negative-sequence currents jeopardizing the security of such schemes. Various restraining techniques or time delay are used in those applications.

7.4 Fault bus schemes

In metal-clad switchgear and in some outdoor installations, the fault bus system for the detection of ground faults can be used. This scheme requires isolating the bus support structure from ground and grounding this structure through a single-point ground and CT as in Figure 39. An overcurrent relay connected to this fault bus CT initiates a trip to all the breakers required to isolate the bus. The maximum effectiveness is obtained by this method when the switchgear is of the isolated phase construction. In this case, the faults always involve ground. Phase-to-phase and three-phase bus faults not involving ground cannot be detected by a fault bus scheme.

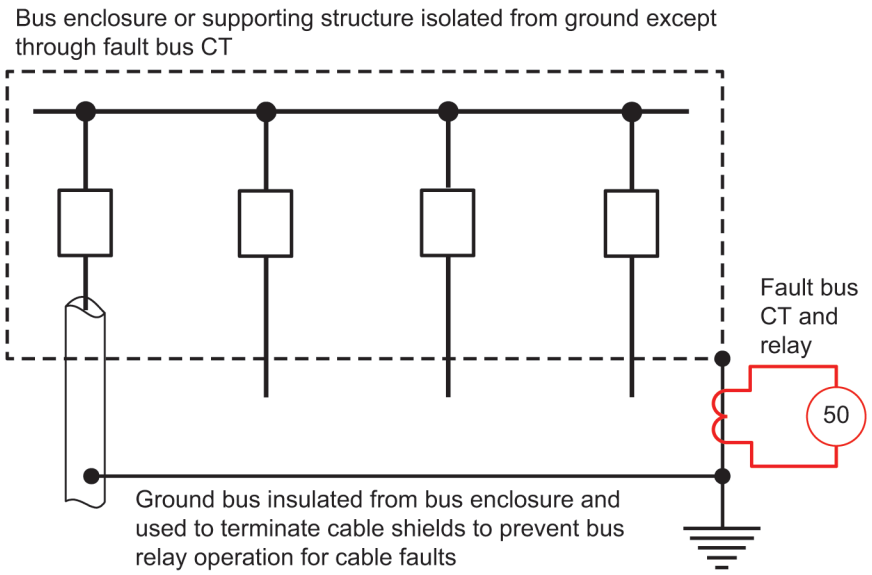

Figure 39—Fault bus relay scheme

For large switchgear, it is desirable to ground the structure at more than one point, each through a CT. The secondaries of all these CTs are paralleled to the single overcurrent relay. If paralleled, the grounding CTs need to be of the same ratio in order to make the scheme immune to external faults causing circulating ground currents. Since fault currents do not flow in this fault bus CT except for bus ground faults, the protection system can be made very sensitive.

The selectivity of this scheme is imperfect as its measuring zone includes the part of connected power cables enclosed by the switchgear, a zone of overlap with network element protection. False tripping can also occur for faults on auxiliary power systems used for mechanism spring charging motors, cubicle lights, etc. This can be avoided by bringing the auxiliary supply into the switchgear through the ground fault CT so that normal auxiliary system ground faults are self-canceling. By using this supply arrangement to feed switchgear receptacles, nuisance trips from power tools can also be avoided. The trip circuit may be supervised by a relay in the neutral or the station's ground relay current polarizing circuit to prevent false tripping from the accidental grounding of power tools, etc. Where unsupervised or where there is an overlap in the protected zone, a coordinating time delay is needed.

The fault bus system is applicable to new installations where provision can be made for effective isolation from ground. Existing installations may not be adaptable due to alternate paths for ground fault current in concrete reinforcing rods or structural steel. Maintenance operations may involve isolating the single-point ground. If the ground is interrupted (for example, to test the integrity of the switchgear ground isolation), a fault on energized equipment could elevate the entire switchgear assembly to primary voltage.

It is necessary to insulate cable sheaths from the switchgear enclosure. An external flashover on a cable entrance bushing may cause improper operation unless the bushing support is insulated from the structure and independently grounded.

It is important to note that the bus structure insulation system is carefully maintained. A dirty or contaminated insulator would allow ground fault current to bypass the fault bus CT, compromising the integrity of the scheme. Also, inadvertent paths to ground caused by, for example, metallic material laid against the fault bus enclosure, may desensitize or disable the fault bus scheme.

Freestanding column CTs and live tank breakers subject to ground faults can also be protected in a similar manner as previously described. Passing the grounding of the CT/breaker column through a CT, which detects ground faults to the column CT, provides high-speed ground fault protection (see also 8.14).

8. Applications of various bus protection schemes

8.1 Partial differential protection

8.1.1 Introduction

Both full and partial differential protection schemes combine individual currents according to the differential operating principle. In partial differential schemes, as explained in Clause 5, currents of one or more of the non-source network elements are not included in the current summation, typically, because they do not have adequate or suitable CTs for a complete differential application. This places the unmeasured network element inside the differential measuring zone, with the protection coverage determined by relay sensitivity setting. Typically, an intentional delay is required to provide coordination with that network element.

High-impedance bus differential schemes, given their typically high sensitivity, cannot be used in partial differential applications.

8.1.2 Loads

Figure 40 shows a typical partial differential scheme that contains a load tapped on the bus. The load circuit does not contain CTs, thus preventing load current from being balanced against the source currents in a full differential scheme.

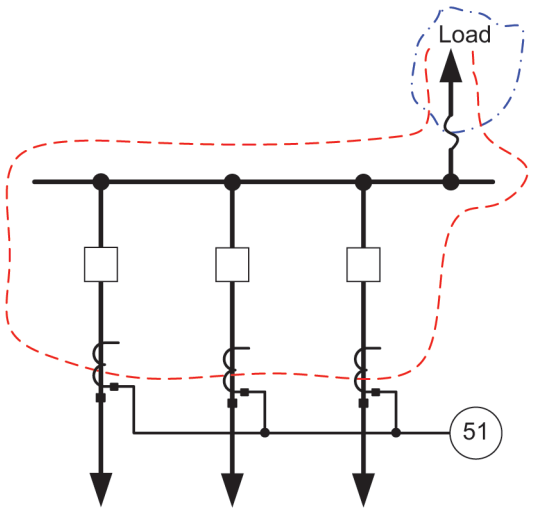

Figure 40—Partial differential protection with a time overcurrent relay

A variety of loads can be directly tapped to a bus, including distribution transformers and substation power transformers. The loads typically have overcurrent protection implemented with fuses or relays. The bus relay is typically desensitized for the load current and delayed to coordinate with the load overcurrent protection devices. Typically, inverse time overcurrent relays are used for partial differential bus protection schemes when coordinating with fuses.

Some loads may be grounded. The bus protection relay is required to account for expected ground current to prevent false tripping. See 8.4 for considerations regarding grounding transformers directly connected to a bus.

The necessity to coordinate the bus relays with the downstream protective devices decreases the bus relay speed. Also, the necessity to set differential pickup above the unmeasured load current may decrease sensitivity.

If current-limiting reactors are used in the load circuits or the unmeasured tap is a bus connected power transformer, a distance relay can be used for bus protection instead of the overcurrent relay (Figure 41). The distance relay is set to reach into, but not through, the lowest reactor/transformer impedance. This application does not require selective settings with the load protection and, therefore, avoids the time delay necessary with the overcurrent relays to provide fast and sensitive bus protection. It does require, however, bus voltage to be a part of the bus protection scheme, making it voltage dependent. Using microprocessor-based multifunctional relays, one can apply distance functions under normal conditions and switch to a time overcurrent protection when the voltage becomes unavailable. A distance relay with proper memory or cross-phase polarization can be selected to reliably detect close-in faults (all bus faults would appear as close-in faults in this scheme). With high enough reactance, overcurrent protection can be also applied in a selective way.

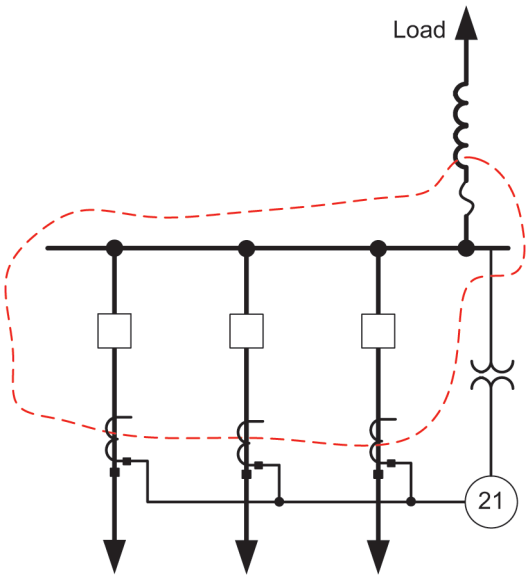

Figure 41—Partial differential protection with a distance relay

If the distance relays are used for bus protection and there are no reactors in the load circuits to provide natural coordination, selectivity with the load-circuit relays may be obtained by adding a time delay to the impedance relay to coordinate with the load protection.

CTs are typically provided on the load to exclude the load circuit from the bus differential protection zone. The applied CT needs to be rated properly for security of the applied bus protection. In particular, its ratio and class are typically selected taking into account bus fault levels and not necessarily the level of the tapped load.

8.1.3 Capacitor banks

As is the situation with loads, a shunt capacitor bank can be included within the bus differential protective zone if CTs are not available on the capacitor bank connection to the protected bus.

The shunt capacitor bank has overcurrent protection implemented with fuses or relays to protect against a major rack fault. When applying a partial differential protection scheme to capacitor banks, it may be desirable to coordinate the bus protection with the capacitor bank protection to avoid tripping the entire bus for capacitor bank faults, depending on bus fault clearing time requirements. This requires a bus differential overcurrent scheme utilizing an inverse time overcurrent relay, as explained in 8.1.2, with respect to bus loads.

If time delayed clearing is not acceptable, a one-shot reclosing scheme can be considered. In this scheme, the bus is tripped high-speed, the capacitor switch is automatically opened, and the bus is reclosed. If the bus holds on a reclose attempt, it is assumed that the fault is on the unmonitored capacitor circuit and the bus is fully restored. This reclosing scheme would also restore the bus for other temporary faults. This scheme might be used in open-air substations with a complex bus arrangement where no branch circuits are lost by the momentary de-energization of the bus. See 8.8 for more discussion on reclosing.

If a shunt capacitor bank is included within a bus partial differential protective zone, the nominal capacitive current needs to be accounted for in the differential relay settings for stability under load conditions.

CTs are typically provided on the capacitor bank connection to exclude it from the bus differential protection zone.

8.2 Combined bus and transformer protection

Protection of power system buses can be implemented by extending the protection zone of equipment adjacent to the bus such that the zone includes the bus. This equipment may be power transformers, combination of power transformers and the low-voltage bus, a tie line to another station, capacitor banks, reactors, or regulators. A typical example is a substation where two transmission or sub-transmission lines supply a step-down transformer, as shown in Figure 42. Typically, the transformer differential relay zone becomes extended and covers the bus zone. A separate restraint winding in the transformer differential relay is connected to each network element. The CT ratings in Figure 42 are typically based on the maximum load current of the lines, the maximum available fault current, and CT secondary burdens. If the power transformer size is small compared with the line rating, the required CT ratio may limit the differential relay sensitivity for transformer faults.

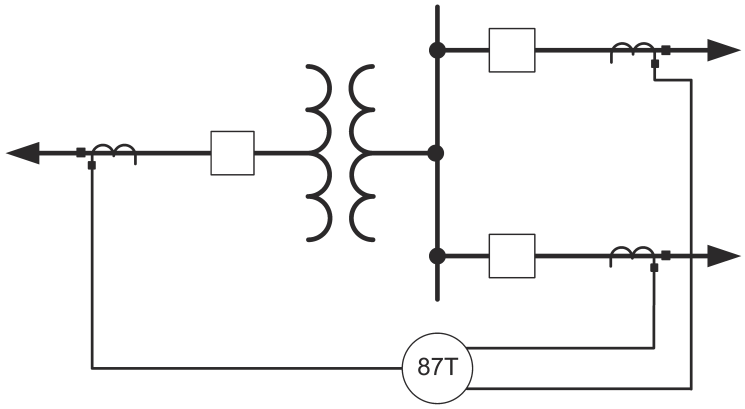

Figure 42—Combined transformer and bus zones

When allowing for the use of the combined differential zone one may consider:

— An outage to all equipment in the protective zone occurs for any fault within the zone.

— Determination of fault location for troubleshooting and repair purposes may be more difficult.