Appendix B
(normative)

Harmonic current limit test

B.1 Test procedure

The procedure shall be as follows:

(a) The inverter shall be connected into a test circuit equivalent to that shown in Figure B.1.

(b) The energy source shall be varied until the a.c. output of the inverter, measured in amperes, lies in the range (100 ± 5) % of the inverter's rated current output.

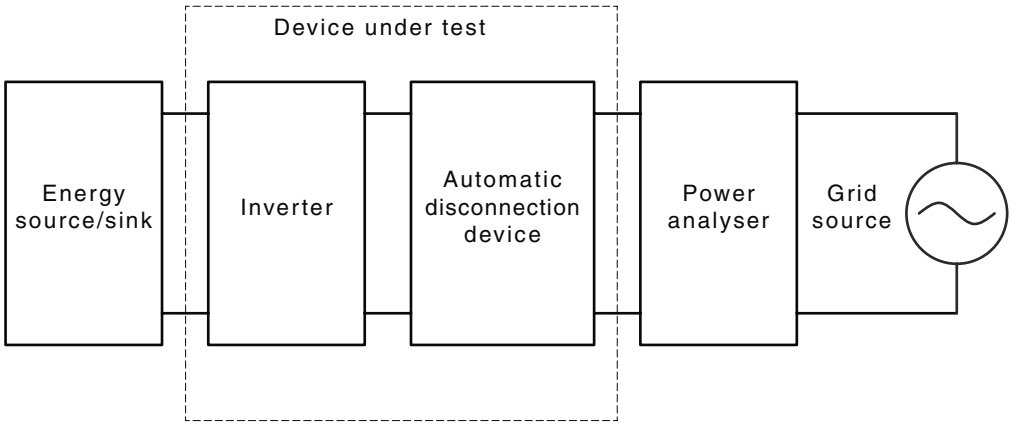
NOTE The required conditions for the grid source are specified in Clause B.3.

(c) The harmonic current content of the inverter output shall be measured and recorded.

(d) The energy source shall be varied until the a.c. output of the inverter, measured in amperes, lies in the range (50 ± 5) % of the inverter's rated current output.

(e) The harmonic current content of the inverter output shall be measured and recorded.

(f) The total impedance of the grid source and reference impedance that simulates a grid shall be in accordance with Appendix A Clause A.6.



NOTE This test circuit applies to a single-phase system. To test a three-phase system, an equivalent three-phase circuit is required.

Figure B.1 — Circuit for power factor test

B.2 Harmonic current limits

When the inverter is tested in accordance with Clause B.1 above, the harmonic currents of the inverter shall not exceed the limits specified in Table 2.2 and Table 2.3 for all points tested.

B.3 Grid source during harmonic test

While the harmonic current measurements are being made, the test voltage at the grid-interactive port of the inverter shall meet the following requirements:

(a) The test voltage and frequency shall be maintained at the grid test voltage.

(b) In the case of a three-phase supply, the angle between the fundamental voltages of each pair of phases shall be maintained at 120° ± 1.5°.

(c) The impedance of the supply source shall be as specified in Clause A.6.

(d) The harmonic ratios of the grid test voltage shall not exceed the limits specified in Table B.1.

Table B.1 — Voltage harmonic limits of test grid

Harmonic order number	Limit based on percentage of fundamental
3	0.9 %
5	0.4 %
7	0.3 %
9	0.2 %
Even harmonics 2–10	0.2 %
11–50	0.1 %
Total harmonic distortion (to the 50th harmonic)	5 %

B.4 Test report

The measured values for harmonic current shall be reported in a table format for each point measured. The table shall contain all measured harmonic components as a current reading and as a percentage of the fundamental with a comparison against the limit for the component. Table B.2 is an example.

The test report shall also include —

(a) the reference impedance value used for the test circuit; and

(b) the background voltage harmonics present at the time of the test.

Table B.2 — Example of table for reporting harmonic limits

Component	Limit	50 % of rated current			100 % of rated current		
	% of fundamental	Value A	Angle degrees	% of fundamental	Value A	Angle degrees	% of fundamental
0	0.5 %						
1	100 %						
2	1 %						
3	4 %						
4	1 %						
5	4 %						
6	1 %						
7	4 %						
8	1 %						
9	2 %						
10	0.5 %						
11	2 %						
12	0.5 %						
13	2 %						
14	0.5 %						
15	1 %						
16	0.5 %						
17	1 %						
18	0.5 %						
19	1 %						
20	0.5 %						
21	0.6 %						
22	0.5 %						
23	0.6 %						
24	0.5 %						
25	0.6 %						
26	0.5 %						
27	0.6 %						
28	0.5 %						
29	0.6 %						
30	0.5 %						
31	0.6 %						
32	0.5 %						
33	0.6 %						
Total harmonic distortion (to 50th component)							

Appendix C
(normative)

Transient voltage limit test

C.1 General

The purpose of this test is to determine that the inverter complies with the transient voltage limits specified in Clause 2.9 when the grid is disconnected from the inverter.

For inverters with rated apparent power not more than 5 kVA, the test load shall be as described in Figure C.1 with the resistor value (R) indicated. For all other inverters, the resistor value (R) shall be calculated such that the total resistive load connected per phase is equivalent to 0.1 % of the rated apparent power of the inverter.

NOTE When choosing a resistor value, the resistive load may be calculated based on the nearest standard resistor value which results in similar load value, as long as the resistive load is within 20 % of the required value.

C.2 Test procedure

The procedure shall be as follows:

(a) The inverter shall be placed in a test circuit equivalent to that shown in Figure C.1, with modification of the resistor value (R) if required (see Clause C.1).

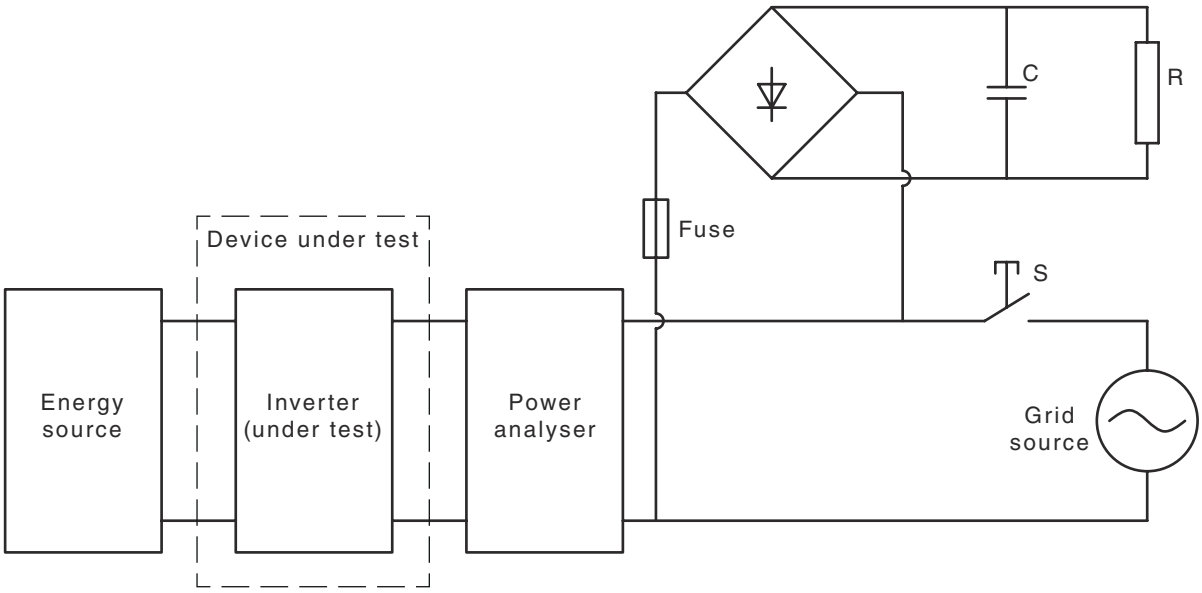
(b) Before the switch is opened, the voltage at the grid-interactive port of the inverter shall be maintained at the grid test voltage.

(c) The energy source shall be varied until the apparent power output of the inverter equals (10 ± 5) % of its rated apparent power.

(d) The switch (S) shall be opened.

(e) The voltage across the grid-interactive port of the inverter shall be recorded at a sample frequency of at least 10 kHz.

(f) Steps (b) to (e) shall be repeated with the inverter operating at (50 ± 5) % and (100 ± 5) % of its rated apparent power.



Key
C = 100 µF
R = 560 kΩ using symbols as shown in Figure

NOTE This test circuit applies to a single-phase system. To test a three-phase system, an equivalent three-phase circuit is required.

Figure C.1 — Circuit for transient voltage limit test

C.3 Transient voltage limits

When tested in accordance with Clause C.2, the voltage-duration curve shall be derived from the measurements sampled for the a.c. voltage at the grid-interactive port.

A voltage-duration curve shall be calculated using the sampled instantaneous voltage over the complete trip time of the inverter. For each voltage (maximum voltage step 10 V), the number of samples greater than that voltage are counted. This number is then multiplied by the sample interval to derive the duration for that voltage. The voltage-duration curve is the locus of all points derived from this process. The inverter is deemed to conform to the transient voltage limit test if the derived voltage-duration curve lies beneath the curve of Figure 2.2 at all points.

The values obtained shall not exceed the limits specified in Table 2.4.

C.4 Test report

The results recorded shall be provided in tabular and graphical formats.

Appendix D
(normative)

DC injection test

D.1 General

The purpose of this test is to verify that the inverter complies with the d.c. current injection limit specified in Clause 2.10 when it connects to the grid. This test is required for inverters that do not incorporate a mains frequency isolating transformer either internally or externally.

The inverter shall be placed in a test circuit equivalent to that shown in Figure B.1. For three-phase systems, current shall be measured in each phase conductor. For single-phase inverters, either the active or neutral current may be measured.

If used, the simulated test grid shall meet the requirements of Appendix A and shall have negligible d.c. offset before the test commences.

D.2 Test procedure

The procedure shall be as follows:

(a) Operate the inverter at 20 % of its rated current and at rated power factor. The inverter shall operate for at least 5 min prior to taking any test measurements (or until the inverter temperature stabilizes). The inverter shall operate at the specified current for the period of the measurement

(b) At the inverter output, measure the r.m.s. voltage, r.m.s. current, and d.c. component (frequency less than 1 Hz) of current on all phases. The average value of 180 consecutive readings of the d.c. component with a measurement period of 1 s for each reading shall be calculated. The average of the 180 consecutive readings for the inverter shall be below the limit specified in Clause 2.10. For each 1 s sample, the absolute value (i.e. unsigned value) shall be used to calculate the 180 s average.

(c) Repeat Steps (a) and (b) with the inverter operating at 60 % and 100 % of its rated current.

(d) Divide the calculated average values for the magnitude of the d.c. component of current by the rated current of the inverter and derive the value of the d.c. current injection as a percentage. This shall be done for 3 test points (20 %, 60 % and 100 %) and for each phase and/or neutral measurement. Record the final calculated values as the percentage of d.c. current injection for each phase.

D.3 DC current limits

All d.c. current injection levels, calculated as percentages, shall be within the limit specified in Clause 2.10.

The resolution of the d.c. component measurement shall be 1 mA or 5 % of the applicable limit, whichever is greater, as specified in Clause 2.10.

D.4 Test report

The measured values shall be reported in a table format for 20 %, 60 % and 100 % of the rated current. Table D.1 is an example.

Table D.1 — Example reporting table for d.c. injection test

Value		20 %	60 %	100 %
Inverter current, A	Setting			
	Actual			
Limit	0.5 % × I_{rated}			
Result	A			
Compliance	(P/F)			

Appendix E
(normative)

Demand response mode testing including disconnection on external signal

E.1 General

The purpose of the tests set out in this Appendix is to verify that the demand response modes respond as required and that the performance of the anti-islanding protection is not affected when these modes are enabled or disabled.

NOTE The Demand Response provisions in this Standard follow the framework in the AS/NZS 4755 series Demand response capabilities and supporting technologies for electrical products.

E.2 Test procedures

E.2.1 Test for demand response and disconnection on external signal

The test system shall be as follows:

(a) The inverter shall be connected into a test circuit equivalent to that shown in Figure B.1.

(b) The voltage shall equal the grid test voltage.

(c) The inverter DRED connection (i.e. terminal block or RJ45 socket) shall be connected to a DRED though an auxiliary DRED test circuit, as shown in Figure E.1.

(d) When measured from the inverter DRED connection point, and with less than 30 mA (a.c. or d.c.) current flow, each DRED switch (S1–S8) and auxiliary DRED test circuit switch (S0) shall have a voltage drop of less than 0.1 V when “on”.

(e) When measured from the inverter DRED connection point, and with less than 30 mA (a.c. or d.c.) current flow, the auxiliary DRED test circuit shall have a voltage drop of 1.5–1.6 V (a.c. or d.c.) between terminals REF GEN/0 and DRM1/5 and COM LOAD/0 and DRM1/5, when auxiliary switches S5a and S1a respectively are “on”.

(f) Switch S9 (see Figure E.1) shall be closed prior to the commencement of each of tests in Clauses E.2.2, E.2.3 and E.2.4.

E.2.2 Test for disconnection at rated power output

The procedure shall be as follows:

(a) The energy source or inverter set-point shall be varied until the a.c. output of the inverter equals (100 ± 5) % of its rated power output.

(b) A signal corresponding to DRM 0 shall be asserted and the time for the device under test to disconnect shall be measured and recorded.

(c) Where the inverter supports the provision of d.c. power to the DRED, power to the DRED shall remain after the automatic disconnection device has operated.

(d) The disconnect signal (DRM 0) shall be removed and the inverter shall be allowed to automatically reconnect (see Clause 4.6).

(e) Switch S9 (see Figure E.1) shall be opened and the time for the device under test to disconnect shall be measured and recorded. See Clause 3.2.2(d).

E.2.3 Test for standard operation of generator demand response modes

The procedure shall be as follows:

(a) All DRM signals shall be removed and the energy source or inverter set-point shall be varied until the a.c. output of the inverter equals (100 ± 5) % of its rated power output. The DRM 3 and DRM 7 reactive power limits shall be set to their maximum allowed values (see Clause 3.2).

(b) A signal corresponding to DRM 7 shall be asserted and DRM 7 response assessed over a period of 2 min in accordance with the requirements of Table E.1.

(c) A signal corresponding to DRM 6 shall be asserted and simultaneous DRM 6 and DRM 7 response assessed over a period of 2 min in accordance with the requirements of Table E.1.

(d) The DRM 7 signal shall be halted and DRM 6 response assessed over a period of 2 min in accordance with the requirements of Table E.1.

(e) A signal corresponding to DRM 5 shall be asserted and DRM 5 response assessed over a period of 4 min in accordance with the requirements of Table E.1.

(f) All DRM signals shall be removed and the energy source or inverter set-point shall be varied until the a.c. output of the inverter equals (50 ± 5) % of the inverter's rated power output and is in a state able to respond to DRM 8.

(g) A signal corresponding to DRM 8 shall be opened and DRM 6 response assessed over a period of 2 min in accordance with the requirements of Table E.1.

E.2.4 Test for standard operation of load demand response modes (such as for battery charging)

The procedure shall be as follows:

(a) All DRM signals shall be removed and the energy source or inverter set-point shall be varied until the a.c. draw of the inverter equals 100 % of the inverter's rated power input. DRM 3 and DRM 7 reactive power limits shall be set to their maximum allowed values (see Clause 3.2).

(b) A signal corresponding with DRM 3 shall be asserted and DRM 3 response assessed over a period of 2 min in accordance with the requirements of Table E.1.

(c) A signal corresponding with DRM 2 shall be asserted and simultaneous DRM 2 and DRM 3 response assessed over a period of 2 min in accordance with the requirements of Table E.1.

(d) The DRM 3 signal shall be halted and DRM 2 response assessed over a period of 2 min in accordance with the requirements of Table E.1.

(e) A signal corresponding with DRM 1 shall be asserted and DRM 1 response assessed over a period of 4 min in accordance with the requirements of Table E.1.

(f) All DRM signals shall be removed and the energy source or inverter set-point shall be varied until the a.c. draw of the inverter equals (50 ± 5) % of the inverter's rated power input and is in a state able to respond to DRM 4.

(g) A signal corresponding with DRM 4 shall be opened and DRM 4 response assessed over a period of 7 min in accordance with the requirements of Table E.1.

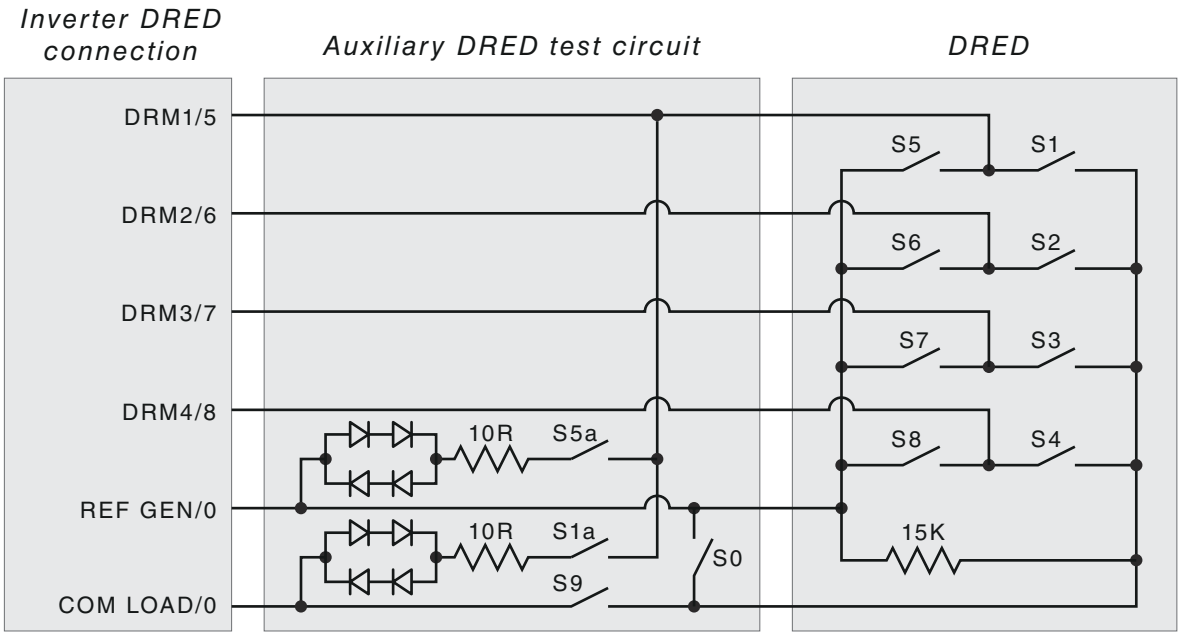


Figure E.1 — DRED connection circuit

E.3 Demand response mode limits

When tested in accordance with Clause E.2, the inverter shall not exceed the active power limits, reactive power limits, or switching time limits specified in Table E.1.

The inverter does not satisfy this test if it —

(a) fails to respond to a DRM instruction of which it is claimed to be capable within the switching time limit;

(b) does not operate in accordance with the requirements for the DRM of Clause 3.1; or

(c) responds to a DRM instruction of which it is not claimed to be capable.